formed over the first polymeric material and the conductive bump material. Support for this amendment to Claim 1 is found at Page 9, lines 12-13 of the specification of the instant application.

Since the above amendments to Claim 1 do not introduce any new matter into the specification of the instant application, entry thereof is respectfully requested. Pursuant to 37 C.F.R. §1.121, applicants have attached a marked-up version of Claim 1 showing the changes made to the claim by the current amendment. The attachment is captioned as "**MARKED-UP VERSION SHOWING CHANGES MADE**".

Claims 1-20 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over U.S. Patent No. 6,228,678 to Gilleo, et al. ("Gilleo, et al."). Claims 21-22 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by Gilleo, et al.

Concerning the §102(b) rejection, it is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that Claims 21-22 of the present application are not anticipated by the disclosure of Gilleo, et al. since the applied reference does not disclose applicants' claimed method recited in Claim 21 wherein the initial semiconductor wafer includes

conductive bump material formed thereon prior to forming the underfill material on the wafer. Specifically, Gilleo, et al. do not disclose a method which includes the steps of:

forming a first polymeric material on a surface of a semiconductor wafer having conductive bump material disposed on portions thereof and removing a portion of said first polymeric material so as to expose top surfaces of said conductive bump material.

Gilleo, et al. provides a method wherein underfill material 14 is applied to a surface of a wafer *prior to* applying the solder bump material. See Col. 3, lines 24-42; Col. 4, lines 54-55; Col. 8, line 64-Col. 9, line 20; Example 1; and FIGS 1-5. Note that in each of the aforementioned sections of Gilleo, et al. the underfill material 14 is formed on the wafer surface prior to forming bumps 18. Applicants submit that at Col. 1, lines 61-66, Gilleo, et al. disclose that a prior underfill surrounds the periphery of the flip chip and occupies space beneath the chip and between the underside chip and the board *which is not occupied by solder*. This disclosure does not disclose applicants' claimed method recited in Claim 21 wherein the underfill material is applied directly to a wafer containing solder bump material thereon.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Gilleo, et al. Applicants respectfully submit that the instant §102 rejection has been obviated and withdrawal thereof is respectfully requested.

Turning to the obviousness rejection citing Gilleo, et al., applicants respectfully submit that the applied reference does not render applicants' method Claims 1-20 obvious since the prior art does not teach or suggest the sequence of steps recited in amended Claim 1.

Specifically, Gilleo, et al. do not teach or suggest a method which includes the step of forming a second polymeric material *that is partially cured* over said first polymeric material and said conductive bump material. Gilleo, et al. disclose applying a thin coating of a flux material that may be subsequently dried. This drying of the applied flux does not necessarily mean that a partially cured second polymeric material is being formed. Indeed, Gilleo, et al. do not mention that the layer containing the flux is a partially cured layer, and applicants find no motivation whatsoever in the prior art to form a second polymeric material *that is partially cured* over a first polymeric material and a conductive bump material. As such, the method recited in Claims 1-20 is not obvious from the disclosure of Gilleo, et al.

The §103 rejection also fails because there is no motivation in the applied reference which suggest modifying the disclosed method to include applicants' claimed sequence of processing steps recited in amended Claim 1. Thus, there is no motivation provided in the applied reference, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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ATTACHMENT: MARKED-UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please amend Claim 1 to read as follows:

1. (Amended) A method of forming a microelectronic interconnect structure containing a bilayer [undefill] underfill layer comprising the steps of:

(a) forming a first polymeric material on a surface of a semiconductor wafer having interconnect pads disposed thereon;

(b) patterning said first polymeric material to provide openings that expose said interconnect pads;

(c) forming conductive bump material in said openings;

(d) forming a second polymeric material that is partially cured over said first polymeric material and said conductive bump material;

(e) dicing said semiconductor wafer into individual chips; and

(f) bonding at least one of said individual chips to an external substrate, wherein during said bonding said conductive bump material penetrates said second polymeric material and contacts a surface of said external substrate.